REMARKS

Claims 1-27 are pending. Claims 1-27 stand rejected under 35 USC § 103(a). Claims 9 and 20 are cancelled. Applicant appreciates our interview and amended the claims per our discussions. Applicant respectfully traverses the rejections in light of the amendments and the following remarks.

Applicant requests interview

Applicant respectfully requests an interview if it would expedite disposition of the application. The undersigned attorney would welcome and encourage a telephone conference with Examiner at (512) 391-4913.

Claim rejections under 35 USC § 103(a)

Claims 1-27 are pending. Claims 1, 12, and 23 stand rejected under 35 USC § 103(a) as being unpatentable over US Patent 6708273 to Ober in view of US Patent 6970563 to Risling, claims 2-7, 13-18, 24-25, and 27 stand rejected under 35 USC § 103(a) as being unpatentable over Ober in view of Risling and in further view of US Patent 6240513 to Friedman et al., and claims 8-9, 19-20, and 26 stand rejected under 35 USC § 103 as being unpatentable over Ober in view of Risling and in further view of US Patent 6901516 to Howard et al.

To establish a prima facie case of obviousness, the modification or combination must teach or suggest all of Applicants' claim limitations.[1]

The combinations of Ober, Friedman, Risling, and Howard fails to establish a prima facie case of obviousness for independent claims 1, 12, and 23 because the combination fails to teach or suggest all of Applicants' claim limitations. In particular, the combinations fail to teach or suggest a cascaded arrangement of processors and the input and output interfaces to interact to coordinate execution according to a predetermined algorithm, wherein the predetermined algorithm can require compression.

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[1] *In re Royka*, 490 F.2d 981, 985, 180 USPQ 580, 583 (CCPA 1974).

Ober describes an encrypt block and a hash block having inputs and outputs connected to a PCMIA bus 76 and an EMI bus 70. The Office action indicates that Ober discloses an input interface and output interface coupled with processors configured to perform cryptographic operations, including an encrypt block and an hash block.

Risling describes shift registers used to in build a scrambler and a descrambler that can scramble or descramble bits in parallel. The Office action points to figure 2 of Risling as support for a cascaded arrangement of processors. Figure 2 of Risling illustrates a scrambler with a shift register to scramble bits serially on the transmitter side of a transmission medium that transmits data over the medium to a descrambler that utilizes a shift register to descramble bits serially.

Friedman discloses a network security device that compresses as well as encrypts data using a LZS compression algorithm. The Office action indicates that a compression block would be obvious in light of Friedman.

Howard describes a system with a ciphering circuit 13 that comprises a controller, a 3-DES core, an MD5 core, and an SHA-1 core. The Office action indicates that it would be obvious to add a controller to forward information and control the blocks.

With respect to amended claim 1, Ober, Risling, Friedman, and Howard do not individually nor in combination teach or suggest, "**an output interface ...configured ... to direct the data through the system in coordination with the input interface according to the predetermined algorithm, wherein the predetermined algorithm can require compression**." First, Ober does not describe the receipt and forwarding of the control information to processors to operate according to a predetermined algorithm so the Office action rejection cites the controller in Howard. With regards to Howard, because the architecture of Howard is very different (see FIG. 3 of Howard vs. FIG. 6 of the present disclosure), the Office action rejection effectively argues that the presence of a controller in any architecture with an encrypt module and a hash module makes the control functionality within the input and output interfaces of claim 1 obvious. Applicant disagrees because the controller in Howard does not perform the same functionality. The controller in Howard does not comprise an output interface that coordinates with an input interface to direct data through the system. The controller in Howard does not direct data

through a cascaded arrangement of processors as well as out of the system in accordance with a predetermined algorithm. And, amongst other functionality, the controller in Howard does not coordinate processing through data compressing/decompressing, obscuring/deciphering, and hashing in accordance with a predetermined algorithm.

Furthermore, Ober, Risling, Friedman, and Howard do not teach or suggest a plurality of processors that comprise "**a cascaded arrangement, each processor having an input coupled to the input interface and an output coupled to respective inputs of each of the other processors downstream in the arrangement**...." Ober, Risling, Friedman, and Howard do not teach or suggest a plurality of processors that comprise "**a first processor having an output coupled with a first input of a second processor and a first input of a third processor....**" Ober, Risling, Friedman, and Howard do not teach or suggest a plurality of processors that comprise "**the second processor compris[ing] an output coupled with a second input of the third processor ....**" And, among other elements, Ober, Risling, Friedman, and Howard do not teach or suggest **"a first processor having an output coupled with a first input of a second processor and a first input of a third processor; wherein the first processor can be configured to compress uncompressed data and to decompress compressed data...."**

With regards to claims 12 and 23, Ober, Risling, Friedman, and Howard do not individually nor in combination teach or suggest:

> ...directing, by an output interface via coordination_between the input interface and the output interface, the received data through the cascaded arrangement of processors according to the predetermined algorithm, each processor having an input coupled to the received data and an output coupled to respective inputs of each of the other processors downstream in the arrangement, wherein directing the received data through the cascaded arrangement of processors comprises directing the received data through the cascaded arrangement comprising a first processor, a second processor having a first input coupled with the output of the first processor, and a third processor having a first input coupled with the output of the first processor and a second input coupled with the output of the second processor....

First, Ober does not describe the receipt and forwarding of the control information to processors to operate according to a predetermined algorithm so the Office action

rejection cites the controller in Howard. With regards to Howard, because the architecture of Howard is very different (see FIG. 3 of Howard vs. FIG. 6 of the present disclosure), the Office action rejection effectively argues that the presence of a controller in any architecture with an encrypt module and a hash module makes the process of claims 12 and 23 obvious. Applicant disagrees because the controller in Howard clearly does not perform the same process.

Ober, Risling, Friedman, and Howard do not teach or suggest **directing by an output interface via coordination between the input interface and the output interface**. Ober, Risling, Friedman, and Howard do not teach or suggest **directing the received data through the cascaded arrangement of processors according to the predetermined algorithm**. Ober, Risling, Friedman, and Howard do not teach or suggest directing the received data **through the cascaded arrangement of processors ... wherein each processor has an input coupled to the received data and an output coupled to respective inputs of each of the other processors downstream in the arrangement**. And, amongst other functionality, Ober, Risling, Friedman, and Howard do not teach or suggest **directing the received data through the cascaded arrangement comprising a first processor, a second processor having a first input coupled with the output of the first processor, and a third processor having a first input coupled with the output of the first processor and a second input coupled with the output of the second processor**.

Furthermore, Ober, Risling, Friedman, and Howard do not teach or suggest:

> performing, by the cascaded arrangement of processors, respective cryptographic operations defined by the predetermined algorithm on the received data using the plurality of processors, wherein the predetermined algorithm defines performance of at least one cryptographic operation from a group of cryptographic operations comprising compressing or decompressing the received data, obscuring or deciphering the received data, and hashing the received data....

Specifically, Ober, Risling, Friedman, and Howard do not teach or suggest "**performing[] by the cascaded arrangement of processors**...." And, among other elements, Ober, Risling, Friedman, and Howard do not teach or suggest "**performing... respective cryptographic operations defined by the predetermined algorithm on the**

received data, wherein the predetermined algorithm defines performance of at least one cryptographic operation from a group of cryptographic operations comprising compressing or decompressing the received data, obscuring or deciphering the received data, and hashing the received data"

Applicant respectfully traverses these rejections of claims dependent upon claims 1, 12, and 23, requests the rejections be withdrawn, and requests that all claims be allowed.

CONCLUSION

Applicant respectfully traverses the cited references with regards to the claim rejections under 35 USC § 103. Accordingly, Applicant believes that this response constitutes a complete response to each of the issues raised in the Office action. In light of the accompanying remarks, Applicant believes that the pending claims are in condition for allowance. Thus, Applicant requests that the rejections be withdrawn, pending claims be allowed, and application advance toward issuance.

A petition and fee for an extension of time accompany this action. No other fee is believed due with this paper. However, if any fee is determined to be required, the Office is authorized to charge Deposit Account 50-0563 for any such required fee.

Respectfully Submitted,

July 2, 2008 /Jeffrey S. Schubert/

Date

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